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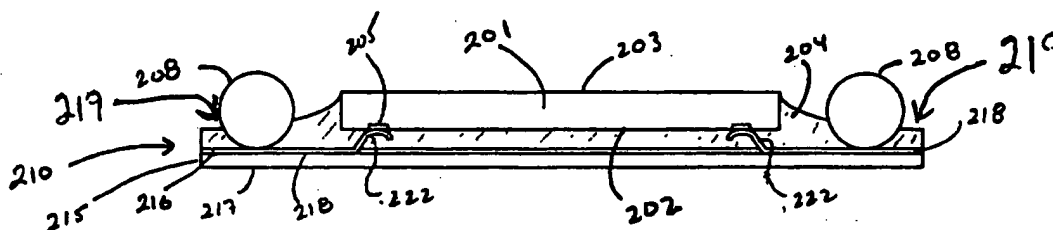
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(54) Title: **STACKED CHIP ASSEMBLY WITH STIFFENING LAYER**



(57) Abstract: A microelectronic subassembly 210 includes a substrate 215 having a top surface 216 and at least one peripheral region 219, a microelectronic element 201 mounted over the substrate 215, a plurality of leads 218, 222 electrically connected to the microelectronic element 201 having outer ends overlying the at least one peripheral region 219 of the substrate 215, and vertical conductors 208 electrically connected with the outer ends of the leads. The subassembly includes an encapsulant layer 204 provided over the top surface 216 of the substrate 215 and around the microelectronic element 201 and the vertical conductors 208 for stiffening the substrate 215 at the at least one peripheral region 219 of the substrate for facilitating handling and testing of the subassembly.

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STACKED CHIP ASSEMBLY WITH STIFFENING LAYER

Technical Field

The present invention generally relates to stacked microelectronic assemblies, and more particularly relates to stacked microelectronic assemblies having a stiffening layer.

Background Art

In certain preferred embodiments of commonly assigned U.S. Patent 5,861,666, the disclosure of which is hereby incorporated by reference herein, a stacked microelectronic assembly includes a plurality of chip and interposer subassemblies. Each subassembly has a circuitized interposer and a semiconductor chip, one face of which confronts a surface of the interposer. Each interposer has at least one peripheral region projecting laterally beyond an edge of the chip mounted to the interposer. Each interposer also includes a plurality of leads electrically connected to contacts on the chip face that extend to the peripheral region of the interposer. The subassemblies are stacked one atop another in a generally vertical configuration so that the chips overlie one another and so that the projecting portions of the interposers overlie one another. The subassemblies are electrically connected one to another by vertical conductors extending alongside the chips and interconnecting the leads of the various interposers at their peripheral regions.

FIG. 1A shows a microelectronic assembly 100 disclosed in U.S. Patent 5,861,666 made from a number N of prefabricated subassemblies, comprising $N-1$ subassemblies 110 and base subassembly 120. Subassembly 110 comprises a semiconductor chip 101 having opposed surfaces 102 and 103, one surface having exposed electrical contacts (not shown), and an interposer 115 having a first surface 116 and a second surface 117. Interposer 115 is preferably a flexible sheet-like element. Chip 101 is mounted on first surface 116 of interposer 115 and the contacts are electrically connected to conductors (not shown) on a surface of interposer 115. Fan-out connectors 111, such as high-melting temperature solder balls, are affixed to the second surface 117 of the interposer

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115 (the side opposite chip 101). In each subassembly 110, the electrical connections between chip 101 and interposer 115 are encapsulated in a material 104 such as an epoxy or elastomer, which fills the gaps between chip 101 and surface 116 and partially surrounds the chip. The base subassembly 120 comprises an encapsulated microelectronic element 101, encapsulant 104 and interposer 125 similar to those described above for subassembly 110. A plurality of joining units 121 are affixed to second surface 127 (the side opposite from microelectronic element 101) of interposer 125. Base subassembly 120 is adapted to serve as the bottom-most unit of stack 100 and may be affixed directly to an external element such as a printed circuit board or a second microelectronic assembly.

When subassemblies 110 and 120 are stacked, fan-out connectors 111 electrically interconnect the subassemblies within the stack, thereby acting as vertical conductors. To allow stacking, fan-out connectors 111 of each subassembly 110 must be positioned outside of the region of interposer 115 of the next lower subassembly occupied by chip 101 and encapsulant 104. Typically, this requirement results in fan-out connectors 111 of each subassembly 110 being disposed in a peripheral region of interposer 115 which is not covered by encapsulant 104 on first surface 116. This peripheral region, therefore, remains quite flexible, which may lead to difficulties in handling the subassemblies and in bonding the fan-out connectors when the subassemblies are stacked. The subassemblies can be made more rigid by dispensing additional encapsulant as shown in FIG. 2A. Increasing the area covered by encapsulant reduces the area available for the fan-out connectors, thereby decreasing the number of rows of connectors that may be used and resulting in poor utilization of the interposer. The problems arising from excessive flexing of the peripheral regions are even more pronounced where multiple rows of fan-out connectors or joining units are employed (FIG. 2B) and where a differently sized die is used in the upper subassemblies (FIG. 2C).

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In spite of the advances set forth in U.S. Patent 5,861,666, there remains a need for a stackable microelectronic subassembly that is easily handled and tested during making of a stacked microelectronic assembly. There also remains a need for a stackable microelectronic subassembly having a stiffening layer for stiffening peripheral regions of the subassembly. The present invention addresses these needs.

Summary of the Invention

In accordance with certain preferred embodiments of the present invention, a microelectronic subassembly includes a substrate, such as a flexible dielectric substrate, having a top surface and at least one peripheral region, a microelectronic element mounted over the substrate, and a plurality of leads electrically connected to the microelectronic element having outer ends overlying the at least one peripheral region of the substrate. The subassembly also desirably includes vertical conductors, such as solder balls, electrically connected with the outer ends of the leads, and an encapsulant layer provided over the top surface of the substrate and around the microelectronic element and the vertical conductors for stiffening the substrate at the at least one peripheral region of the substrate. In certain embodiments, the substrate may be a flexible substrate made of a polymeric material.

In certain preferred embodiments, the microelectronic element is a semiconductor chip having a front face with contacts and a back face remote therefrom. The semiconductor chip may be assembled with the substrate so that the front face of the semiconductor chip faces the top surface of the substrate with the leads connected to the chip contacts. In other preferred embodiments, the semiconductor chip may be assembled with the substrate so that the back face of the semiconductor chip confronts the top surface of the substrate and the front face faces away from the substrate. In this particular embodiment, the subassembly may include conductive wires having first ends connected to the chip contacts and second ends connected to the leads.

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The subassembly also preferably includes a compliant layer disposed between the microelectronic element and the substrate so as to permit relative movement of the microelectronic element and the substrate during thermal cycling of the subassembly. The compliant layer may include a plurality of compliant pads spaced from one another for defining channels or gaps therebetween. The stiffening encapsulant layer may be disposed in the channels between the compliant pads.

The stiffening encapsulant layer is preferably selected from the group consisting of flexibilized epoxies, silicone elastomers, glass sheet, glass-filled epoxies, ceramic materials and plastics. Although the present invention is not limited by any particular theory of operation, it is believed that providing a stiffening layer that surrounds the vertical conductors in the peripheral region of the substrate will enhance handling and testability of the subassembly by providing sufficient stiffness in the peripheral region of the subassembly. Absent the stiffener layer, the peripheral region of the substrate may flex, bend or flop to an undesirable degree during testing and handling.

In certain preferred embodiments, the substrate includes a plurality of dielectric layers, and a plurality of layers of conductive traces extending through the substrate. The substrate may also include a conductive metal layer adapted to function as a power plane. In yet other preferred embodiments, the substrate may also include a conductive metal layer adapted to function as a ground plane.

In other preferred embodiments of the present invention, a microelectronic subassembly includes a substrate having a top surface, a bottom surface and at least one peripheral region, a microelectronic element mounted over the top surface of the substrate, and a plurality of leads electrically connected to the microelectronic element, the leads having outer ends overlying the at least one peripheral region of the substrate. The microelectronic subassembly also preferably includes vertical conductors electrically connected with the outer ends of the leads, and an encapsulant layer provided

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over one of the surfaces of the substrate and around the vertical conductors for stiffening the at least one peripheral region of the substrate. In certain preferred embodiments, the vertical conductors are disposed over the bottom surface of the substrate and the stiffening encapsulant layer is provided over the bottom surface of the substrate and around the vertical conductors.

In yet further preferred embodiments of the present invention, a microelectronic assembly includes a plurality of microelectronic subassemblies, each subassembly having a substrate with at least one peripheral region, a microelectronic element mounted over the substrate, a plurality of leads electrically connected to the microelectronic element having outer ends overlying the at least one peripheral region of the substrate, vertical conductors electrically connected with the outer ends of the leads, and an encapsulant layer provided over a surface of the substrate and around the vertical conductors for stiffening the substrate at the least one peripheral region of the substrate. The microelectronic subassemblies are stacked one atop another and electrically interconnected through the vertical conductors. The vertical conductors preferably form electrical interconnections between leads of different subassemblies. The vertical conductors preferably include metallic masses, such as solder balls. The microelectronic elements of the assembly may vary in size.

In certain preferred embodiments, each of the substrates has a central region aligned with the microelectronic element mounted thereto and a plurality of peripheral regions extending outwardly at a plurality of edges of the substrate.

These and other preferred embodiments of the present invention will be described in more detail below.

Brief Description of the Drawings

FIG. 1A shows a conventional stacked microelectronic assembly.

FIG. 1B shows an upper layer of the stacked microelectronic assembly of FIG. 1A.

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FIG. 1C shows a base layer of the stacked microelectronic assembly of FIG. 1A.

FIG. 2A shows another conventional stacked microelectronic assembly.

FIG. 2B shows still another conventional stacked microelectronic assembly.

FIG. 2C shows yet another conventional stacked microelectronic assembly.

FIG. 3A shows a stacked microelectronic assembly including stiffening layers, in accordance with certain preferred embodiments of the present invention.

FIG. 3B shows an upper layer of the stacked microelectronic assembly of FIG. 3A.

FIG. 3C shows a base layer of the stacked microelectronic assembly of FIG. 3A.

FIG. 4A shows an enlarged fragmentary view of the stacked microelectronic assembly of FIG. 3A.

FIG. 4B shows another enlarged fragmentary view of FIG. 4A in accordance with certain preferred embodiments of the present invention.

FIG. 4C shows still another enlarged fragmentary view of FIG. 4A.

FIG. 5A shows a stacked microelectronic assembly with stiffening layers, in accordance with yet other preferred embodiments of the present invention.

FIG. 5B shows a stacked microelectronic assembly with stiffening layers, in accordance with further preferred embodiments of the present invention.

FIGS. 6A and 6B show perspective views of a stacked microelectronic assembly with stiffening layers during various phases of the assembly process, in accordance with certain preferred embodiments of the present invention.

FIG. 7A shows a stacked microelectronic assembly with one or more stiffening layers, in accordance with still other preferred embodiments of the present invention.

FIG. 7B shows an upper subassembly layer of the stacked microelectronic assembly of FIG. 7A.

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FIG. 7C shows a base layer of the stacked microelectronic assembly of FIG. 7A.

FIG. 8 shows a stacked microelectronic assembly with one or more stiffening layers, in accordance with other preferred embodiments of the present invention.

FIG. 9 shows a stacked microelectronic assembly with one or more stiffening layers, in accordance with still other preferred embodiments of the present invention.

FIG. 10 shows a stacked microelectronic assembly with stiffening layers, in accordance with still further preferred embodiments of the present invention.

Best Mode of Carrying Out Invention

FIG. 3A illustrates a preferred embodiment of the stacked assembly of the present invention. Stacked assembly 200 includes a plurality of $N-1$ subassemblies 210 stacked one atop another with a base subassembly 220 occupying the bottom-most position in the stack. Referring to FIGS. 3B and 3C, each subassembly 210, 220 includes a microelectronic element 201, such as a semiconductor chip, having a front face 202, a back face 203 opposite front face 202 and a plurality of contacts 205 exposed at front face 202. Preferably, contacts 205 are exposed in a peripheral region of the chip face. Interposer 215 is desirably a dielectric element having a first surface 216, a second surface 217 opposite first surface 216 and a plurality of conductive pads (not shown) disposed on first surface 216. Interposer 215 also preferably has conductive elements 218 such as metallic traces thereon, with contacts 205 of chip 201 being electrically connected to conductive elements 218. Preferably, interposer 215 is made of a flexible dielectric material such as polyimide tape. Interposer 215 may also include one or more additional layers such as a conductive metal layer to serve as a power or ground plane, multiple layers of traces and multiple dielectric layers.

Referring to FIGS. 3B and 3C, the electrical connection between the contacts on face surface 202 and the pads on first surface 216 may be made by any of the known methods of making electrical connections including, but not limited to, flip-

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chip bonding, wire bonding, tab bonding and the bonding methods disclosed in commonly assigned U.S. Patents 5,148,265; 5,148,266; 5,518,964 and 5,536,909, the disclosures of which are incorporated herein by reference. Preferably, at least one pad is movable with respect to at least one contact. The preferred embodiments of the present invention are not limited to the illustrated flip-chip configuration where face surface 202 faces first surface 216 of interposer 215. The present invention also contemplates "face-up" configurations, wherein a face surface 202 of a chip faces away from interposer 215. The utilization of lead-bonding methodologies disclosed in the U.S. Patents cited above are preferred because the resulting lead structures allow the formation of subassemblies having a very low overall height.

Referring to FIGS. 3B and 3C, fan-out connectors 208, such as high-melting solder balls, are disposed on first surface 216 of interposer 215 and are electrically connected to at least some of conductive elements 218 on first surface 216. Fan-out connectors 208 are located so that, when subassemblies 210, 220 are stacked one atop another, fan-out connectors 208 electrically interconnect the subassemblies within the stack, acting as vertical conductors. Fan-out connectors 208 are preferably located around outer edges of chip 201 and adjacent peripheral regions of interposer 215.

Subassemblies 210, 220 also include respective stiffening layers 204. Each stiffening layer 204 is preferably made of an encapsulating material, such as a flexibilized epoxy or silicone elastomer, which surrounds both microelectronic element 201 and fan-out connectors 208. The encapsulant also desirably encapsulates the leads or other bonding structures 222 connecting contacts 205 of chip 201 to the conductive elements of interposer 215.

Referring to FIG. 3C, subassembly 220 also preferably includes joining units 228 that are disposed on second surface 217 of interposer 215 and electrically connected to at least some of the pads on first surface 216. Joining units 228 may be used to attach assembly 200 to electrical contacts or pads

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on an external electronic element, such as those on a printed circuit board, or a second microelectronic assembly.

As illustrated in FIG. 4A, a joining unit may be formed by attaching a eutectic solder ball 228 to a conductive pad 229 affixed to second surface 217 of interposer 215. Preferably, peripheral region 206 of interposer 215 is penetrated by vias 226. Vias 226 may be open at both ends or closed at one end to accommodate various methods of making electrical connections, as are known in the art. Vias 226 may be electrically conductive. Referring to FIG. 4B, in certain preferred embodiments, interposer 235 is formed with openings 239 therein, and solder mass 239 is allowed to flow into an opening 238 to establish electrical contact with first surface 236. The embodiment of FIG. 4B allows interposer 235 to be constructed with a single metallic tape at a substantially lower cost than the embodiment of FIG. 4A, for which a bimetallic tape would more typically be employed.

Referring to FIG. 4A, each subassembly preferably includes fan-out connectors 208, such as high-temperature solder balls, bonded to conductive elements 218. The diameter of each connector 208 is greater than the combined thicknesses of compliant layer 212 and microelectronic element 201 so that fan-out connector 208 extends beyond chip 201 to contact via 226 of the subassembly above it. Preferably, back surface 203 of chip 201 is in close proximity to second surface 217 of its adjacent subassembly. A layer 212 of compliant material such as a gel or an elastomer is disposed between front face 202 of each chip 201 and surface 216 of interposer 215. Thus, interposer 215 of each subassembly 210, 220 is mechanically decoupled from chip 201 and free to deform and deflect independent of the chip. Fan-out connectors 208 may be provided as conventional "solid-core solder balls", initially having coatings of solder which reflow to bond the connectors 208 to vias 226 and, preferably, to contact conductive elements 218.

Referring to FIG. 4A, stiffening layer 204 is provided over top surface 216, preferably surrounding microelectronic element 201 and fan-out connector 208. Preferably, stiffening

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layer 204 is formed of an encapsulant, more preferably, of a flexibilized epoxy or silicone elastomer. In certain preferred embodiments, the encapsulant of interposer 215 fills gaps between the front face 202 of chip 201 and top surface 216 of interposer 215, and encapsulates leads 222.

Referring to FIGS. 4A and 4C, microelectronic element 201 is mounted to surface 206 of interposer 215 in a "face-down" arrangement, that is, where the face surface 202 of element 201 confronts surface 206. Leads 222 electrically connect conductive elements 218 to contacts 205. In preferred embodiments, leads 222 are flexible leads, preferably formed of copper, gold, alloys thereof and combinations thereof. For example, leads 222 may be formed according to the methods disclosed in commonly assigned U.S. Patents 5,148,265; 5,148,266; 5,787,581 and 5,977,618. Referring to FIG. 4C, lead 222a initially extends over slot 224. Lead 222a may have a notch or other weakened portion that provides a fracture point 223 in the lead. A tool may be inserted into slot 224 to break lead 222a and push it to the position of lead 222, making contact with a contact 205 on chip face 202.

The embodiment of FIG. 4A can readily be modified for "face-up" configurations, that is, the contact-bearing face of the chip faces away from interposer 215, and that contacts 205 can be electrically connected to terminals on a surface of interposer 215 by wire bonding, flip-chip bonding, tab bonding, or other means of electrical bonding presently known in the art. Moreover, it will be obvious to those skilled in the art that an interposer may be fabricated without a conductive element 218 and that lead 222 may be fabricated so as to electrically connect a terminal on a surface of the interposer to a contact on chip face 202.

Referring to FIG. 4A, each subassembly 210, 220 preferably includes a spacer layer 212 disposed between front face 202 of microelectronic element 201 and interposer 215. Spacer layer 212 is preferably compliant. Preferred materials for the spacer layers 212 include epoxies and silicones, with flexibilized epoxies and silicone elastomers being particularly preferred. Spacer layer 212 may comprise a

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single pad of material, as depicted in FIG. 4A, or a plurality of such pads. The spacer layer 212 absorbs the stress of differential thermal expansion of interposer 215 and the microelectronic element 201 and inhibits deformation of the flexible dielectric structure during handling and installation of the subassembly. Spacer layer 212 is preferably positioned to avoid obstructing movement of flexible leads 222 or interfering with contact between lead 222 and electrical contact 205. In another preferred embodiment of the invention, only the base subassembly 220 of the stacked microelectronic assembly is provided with a compliant spacer layer 212, as the effects of differential thermal expansion typically are most critical at the bottom-most subassembly in the stack.

Referring to FIG. 4A, the individual subassemblies 210, 220 are fabricated as described above. Each subassembly 210, 220 may be tested separately by engaging vias 226 with contacts of a test socket, or by engaging fan-out connector 208 in a socket. The chip 201, leads 222 and connections can then be tested by actual operation of the chip. After testing, the individual subassemblies 210, 220 are stacked one atop another so that chips 201 generally overlie one another in front face to rear face disposition, and so that peripheral regions 206 of the various interposers 215 are aligned with one another. In this arrangement, vias 226 of the various interposers 215 and the fan-out connectors 208 associated therewith are also aligned one with another. Thus, the connector 208 associated with its respective via 226 on one interposer makes contact with a corresponding via 226 on the next interposer in the stack.

Referring to FIG. 4A, joining units 228, such as solder balls, are disposed on second surface 217 of the bottom-most interposer 215 and are electrically connected to at least some conductive elements 218 on first surface 216. Joining units 228 may be used to attach the stacked microelectronic assembly to electrical circuit contacts or pads on a printed circuit board or a second microelectronic assembly.

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Referring to FIG. 6A, microelectronic elements 601 are attached to a strip of interposer 615 and electrically connected to the interposer as described herein, and fan-out connectors 608 are affixed to surface 616 of interposer 615 as described herein. Referring to FIG. 6B, an encapsulant, such as a flexibilized epoxy or silicone elastomer, is provided over top surface 616 of interposer 615 to surround microelectronic element 601 and fan-out connectors 608.

Referring to FIGS. 7A-7C, fan-out connectors 708 are affixed to second surface 717 of interposer 715. Stiffening layer 704 is joined to second surface 717 so as to surround fan-out connectors 708. Stiffening layer 704 includes a depression or opening 705 formed therein so that when subassemblies 710, 720 are stacked one atop another, the respective encapsulated chip 711, 721 of the lower subassembly 711, 721 fits within the opening 705 of the upper assembly. In the embodiment shown, the bottom subassembly 720 in the stack 700 is fabricated without fan-out connectors. Subassembly 720 may be provided with joining units 728 of the types discussed herein for other embodiments of the present invention.

Although FIGS. 3A, 4A and 7A depict embodiments wherein the centers of the microelectronic elements are aligned with each other, the present invention also includes embodiments wherein at least one microelectronic element overlies other microelectronic elements in such a way that the centers of such elements are not aligned. Moreover, the microelectronic elements of the present invention are not limited to single semiconductor chips. Alternatively, a plurality of semiconductor chips may be laid side by side along the first surface of the interposer or stacked one atop another within a subassembly without departing from the invention herein disclosed.

In still other preferred embodiments, other electrically conductive elements may be utilized for creating vertical electrical connections between the subassemblies within a stack. For example, referring to FIG. 4A, vias 226 may serve as fan-out connectors in embodiments where electrically

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conductive vias 226 are aligned one with another, with an electrically conductive rod inserted through the aligned vias 226 to provide the electrical interconnection between the subassemblies. Alternatively, other methods of establishing vertical electrical connections, such as those disclosed in commonly assigned U.S. Patent 5,861,666, may be used without departing from the scope of the invention. In all such embodiments, stiffening layer 204 would be modified as needed to allow electrical connections to be formed according to the connection method used.

The stiffening layer 204 may be may be formed from materials other than the encapsulants discussed herein. For example, suitable materials include, but are not limited to, glass sheet, glass-filled epoxy, ceramic materials, or a plastic sheet, so long as the stiffening layer surrounds the microelectronic elements in the central region of the interposer and the fan-out connectors in the peripheral regions of the interposer. Alternatively, the stiffening layer may be formed from epoxy or elastomer materials that have a modulus different from the modulus of the materials used to encapsulate leads 222 or to form compliant layer 212.

Although the present invention is not limited by any particular theory of operation, it is believed that providing a stiffening layer on the interposer surface creates a subassembly that is more rigid than those fabricated by methods currently in use, but which still provides some flexibility in the subassembly design. A stiffening layer that surrounds the microelectronic element and/or fan-out connectors further increases the rigidity of the resulting structure. The methods of the present invention may be used to fabricate subassemblies with single or multiple rows of overhung fan-out connectors such as the embodiment of FIG. 5A, or with dies of differing sizes, such as the embodiment of FIG. 5B.

Referring to FIGS. 3B and 3C, each subassembly 210, 220 preferably has a height or thickness that is about 1 millimeter or less. In more preferred embodiments, the subassembly has a thickness of about 700 microns or less. The

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preferred lead structures, such as leads 222, have a height of 500 microns or less. Such vertically extensive leads allow the contacts on the chip face to move relative to the pads on the first surface of the dielectric element in response to differences in thermal expansion among the elements of the assembly. The stiffening layer 204 provides the desired stiffness without adding additional height to the subassembly.

The stacked assembly of the present invention can be fabricated using readily available techniques. The assembly preferably provides electrically conductive pathways connecting the chips in the stack to one another and to external circuit elements with low impedance and short circuit path lengths, while minimizing mechanical stresses caused by differences in thermal expansion between the chip and the dielectric elements. The presence of stiffening layers in one or more of the subassemblies result in a more rigid structure than stacked assemblies formed by techniques presently in use.

Referring to FIG. 8, in accordance with another preferred embodiment of the present invention, a stacked microelectronic assembly 800 includes a first subassembly 810 stacked atop and electrically interconnected with a second subassembly 820. The first subassembly includes a flexible substrate 815 having a first surface 816 and a bottom surface 818 remote therefrom. First subassembly 810 also includes conductive elements 818, such as conductive traces provided over the top surface 816 of flexible substrate 815. First subassembly 810 also includes a microelectronic element 801, such as a semiconductor chip, including a front contact bearing face 802 and back face 803 remote therefrom. During assembly, microelectronic element 801 is mounted above the top surface 816 of flexible substrate 815 with back face 803 facing top surface 816. The microelectronic element 801 is electrically interconnected with conductive element 818 by wire bonds 822. Preferably, wire bonds 822 have first ends 823 attached to contacts (not shown) on front face 802 of microelectronic element 801 and second ends 824 attached to conductive element 818. Fan-out connectors 808, such as high-melting temperature solder balls, are disposed on top surface 816 of flexible substrate 815 and

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are electrically connected with at least some of the conductive elements 818 extending over top surface 816. The fan-out connectors 808 are preferably located atop the surface 816 of flexible substrate 815 so that when the subassemblies 810, 820 are stacked one atop another, the fan-out connectors 808 electrically interconnect the subassemblies within the stack, thereby acting as vertical conductors. In preferred embodiments, the fan-out connectors 808 extend beyond the outer edges of the microelectronic element 801. In highly preferred embodiments, the fan-out connectors 808 are located adjacent peripheral regions 825 of the flexible substrate 815.

Subassembly 810 also preferably includes a stiffening layer 804 made of an encapsulating material. In preferred embodiments, the stiffening layer 804 is made of an encapsulating material such as flexibilized epoxy or silicone elastomers, which surround both microelectronic element 801 and fan-out connectors 808. The stiffening layer 804 may also encapsulate the wire bonds 822. In certain preferred embodiments, the stiffening layer completely encapsulates the wire bonds 822 and the microelectronic element 801. In other embodiments, however, such as the one shown in FIG. 8, the stiffening layer encapsulates only certain sections of the wire bond 822.

Stacked microelectronic assembly 800 also includes second subassembly 820 having flexible substrate 815', microelectronic element 801', fan-out connectors 808', wire bonds 822' and stiffening layer 804'. In the particular embodiment shown in FIG. 8, second subassembly 820 is substantially similar to first subassembly 810. As with the first subassembly 810, the stiffening layer 804' of second subassembly 820 adds rigidity to the subassembly in the vicinity of the peripheral region 825' of flexible substrate 815'.

Stacked microelectronic assembly 800 also includes one or more joining units 828' provided over second surface 818' of flexible substrate 815'. The joining units 828' are preferably electrically interconnected to at least some of the fan-out connectors 208 and/or microelectronic elements 801,

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801'. Joining units 828' are preferably used to attach the stacked microelectronic assembly to an external element, such as a substrate having electrical contacts or pads.

FIG. 9 shows a stacked microelectronic assembly 900, in accordance with another preferred embodiment of the present invention, including first subassembly 910 stacked over second subassembly 920. First subassembly 910 includes substrate 915 having top surface 716 and microelectronic element 901 having back face 903 facing top surface 716. The front face 902 faces away from top surface 916 and has contacts (not shown) that are electrically interconnected with conductive elements 919 by wire bonds 922. First subassembly 910 includes fan-out connectors 909 at peripheral regions 925 of flexible substrate 915. First subassembly 910 also includes a stiffening layer 904 that extends around microelectronic element 901 and fan-out connectors 909.

Second subassembly 920 includes microelectronic element 901' having a contact bearing front face 902' that faces top surface 916' of flexible substrate 915'. The mounting of the microelectronic element 901' over flexible substrate 915' is commonly referred to as a "flip-chip" assembly. The microelectronic element 901' is electrically interconnected with conductive elements 919' extending over first surface 916' using flexible leads 922'.

FIG. 10 shows a stacked microelectronic assembly 1000 including a first subassembly 1010 stacked over a second subassembly 1020. First subassembly 1010 includes a microelectronic element 1001 having a contact bearing face 1002 facing away from top surface 1016 of flexible substrate 1015. Microelectronic element 1001 is electrically interconnected with conductive elements 1018 by wire bonds 1022. First subassembly 1010 includes fan-out connectors 1008 provided in peripheral regions 1025 of flexible substrate 1015. A stiffening layer 1004 surrounds microelectronic element 1001 and fan-out connectors 1008 for providing stiffening at peripheral regions 1025 of flexible substrate 1015, thereby facilitating testing and handling of the subassembly..

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Second subassembly 1020 includes generally similar elements as those described above in first subassembly 1010, however, second subassembly 1020 includes a microelectronic element 1001' that is substantially larger than microelectronic element 1001 of first subassembly 1010.

Although the invention herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present invention. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the spirit and scope of the present invention as described herein. Such changes would include the incorporation of features of the stacked microelectronic assemblies disclosed in U.S. Patent 5,861,666 or commonly owned U.S. Patents 6,121,676 and 6,225,688 and commonly assigned U.S. Patent Application Serial No. 09/776,356, the disclosures of which are incorporated herein by reference.

Industrial Applicability

The present invention has applicability in the microelectronics industry.

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CLAIMS:

1. A microelectronic subassembly comprising:
a substrate having a top surface and at least one peripheral region;
a microelectronic element mounted over the substrate;
a plurality of leads electrically connected to the microelectronic element having outer ends overlying the at least one peripheral region of the substrate;
vertical conductors electrically connected with the outer ends of the leads;
an encapsulant layer provided over the top surface of the substrate and around the microelectronic element and the vertical conductors for stiffening the substrate at the at least one peripheral region of the substrate.
2. The subassembly as claimed in claim 1, wherein the substrate is flexible.
3. The subassembly as claimed in claim 2, wherein the flexible substrate comprises a dielectric material.
4. The subassembly as claimed in claim 2, wherein the flexible substrate comprises a polymeric material.
5. The subassembly as claimed in claim 1, wherein the microelectronic element is a semiconductor chip having a front face with contacts and a back face remote therefrom.
6. The subassembly as claimed in claim 5, wherein the front face of the semiconductor chip faces the top surface of the substrate and the leads are connected to the chip contacts.
7. The subassembly as claimed in claim 5, wherein the back face of the semiconductor chip faces the top surface of the substrate, and wherein the subassembly further comprises conductive wires having first ends connected to the chip contacts and second ends connected to the leads.
8. The subassembly as claimed in claim 1, further comprising a compliant layer disposed between the microelectronic element and the substrate so as to permit relative movement of the microelectronic element and the substrate during thermal cycling of the subassembly.

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9. The subassembly as claimed in claim 8, wherein the compliant layer comprises a plurality of compliant pads spaced from one another, the spaced compliant pads defining channels therebetween.

10. The subassembly as claimed in claim 9, wherein the stiffening encapsulant layer is disposed in the channels between the compliant pads.

11. The subassembly as claimed in claim 1, wherein the stiffening encapsulant layer is selected from the group consisting of flexibilized epoxies, silicone elastomers, glass sheet, glass-filled epoxy, ceramic materials and plastic.

12. The subassembly as claimed in claim 1, wherein the substrate comprises a plurality of dielectric layers, and wherein a plurality of layers of conductive traces extend through the substrate.

13. The subassembly as claimed in claim 1, wherein the substrate includes a conductive metal layer adapted to function as a power plane.

14. The subassembly as claimed in claim 1, wherein the substrate includes a conductive metal layer adapted to function as a ground plane.

15. A microelectronic subassembly comprising:

- a substrate having a top surface, a bottom surface and at least one peripheral region;

- a microelectronic element mounted over the top surface of the substrate;

- a plurality of leads electrically connected to the microelectronic element having outer ends overlying the at least one peripheral region of the substrate;

- vertical conductors electrically connected with the outer ends of the leads;

- an encapsulant layer provided over one of the surfaces of the substrate and around the vertical conductors for stiffening the at least one peripheral region of the substrate.

16. The subassembly as claimed in claim 15, wherein the vertical conductors are disposed over the bottom surface of the substrate.

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17. A microelectronic assembly including a plurality of microelectronic subassemblies, each the subassembly comprising:

- a substrate having at least one peripheral region;
- a microelectronic element mounted over the substrate;

- a plurality of leads electrically connected to the microelectronic element having outer ends overlying the at least one peripheral region of the substrate;

- vertical conductors electrically connected with the outer ends of the leads;

- an encapsulant layer provided over a surface of the substrate and around the vertical conductors for stiffening the substrate at the at least one peripheral region of the substrate, wherein the microelectronic subassemblies are stacked one atop another and electrically interconnected through the vertical conductors.

18. The microelectronic assembly as claimed in claim 17, wherein the substrates are flexible dielectric substrates.

19. The microelectronic assembly as claimed in claim 17, wherein the vertical conductors form interconnections between leads of different subassemblies.

20. The microelectronic assembly as claimed in claim 17, wherein the vertical conductors comprise metallic masses.

21. The microelectronic assembly as claimed in claim 20, wherein each the substrate has a central region aligned with the microelectronic element mounted to such flexible substrate and a plurality of peripheral regions extending outwardly at a plurality of edges of each such substrate.

22. The microelectronic assembly as claimed in claim 17, wherein the microelectronic element is a semiconductor chip having a front face with contacts and a back face remote therefrom.

23. The microelectronic assembly as claimed in claim 22, wherein the front face of the semiconductor chip faces a top surface of the substrate and the leads are connected to the chip contacts.

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24. The microelectronic assembly as claimed in claim 22, wherein the back face of the semiconductor chip faces a top surface of the substrate and wherein the subassembly further comprises conductive wires having first ends connected to the chip contacts and second ends connected to the leads.

25. The microelectronic assembly as claimed in claim 17, further comprising a compliant layer disposed between the microelectronic element and the substrate so as to permit relative movement of the microelectronic element and the substrate during thermal cycling of the subassembly.

26. The microelectronic assembly as claimed in claim 25, wherein the compliant layer comprises a plurality of compliant pads spaced from one another for defining channels therebetween.

27. The microelectronic assembly as claimed in claim 26, wherein the stiffening encapsulant layer is disposed in the channels between the compliant pads.

28. The microelectronic assembly as claimed in claim 17, wherein the stiffening encapsulant layer is provided around outer edges of the microelectronic element.

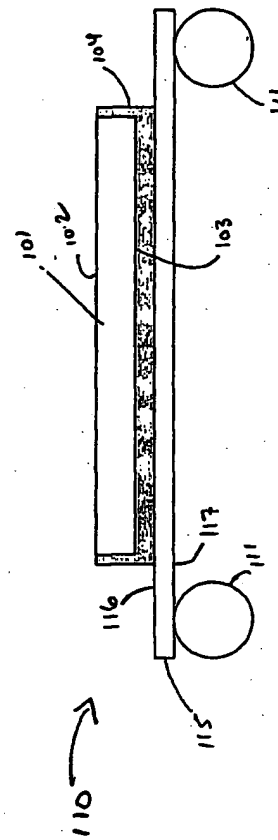
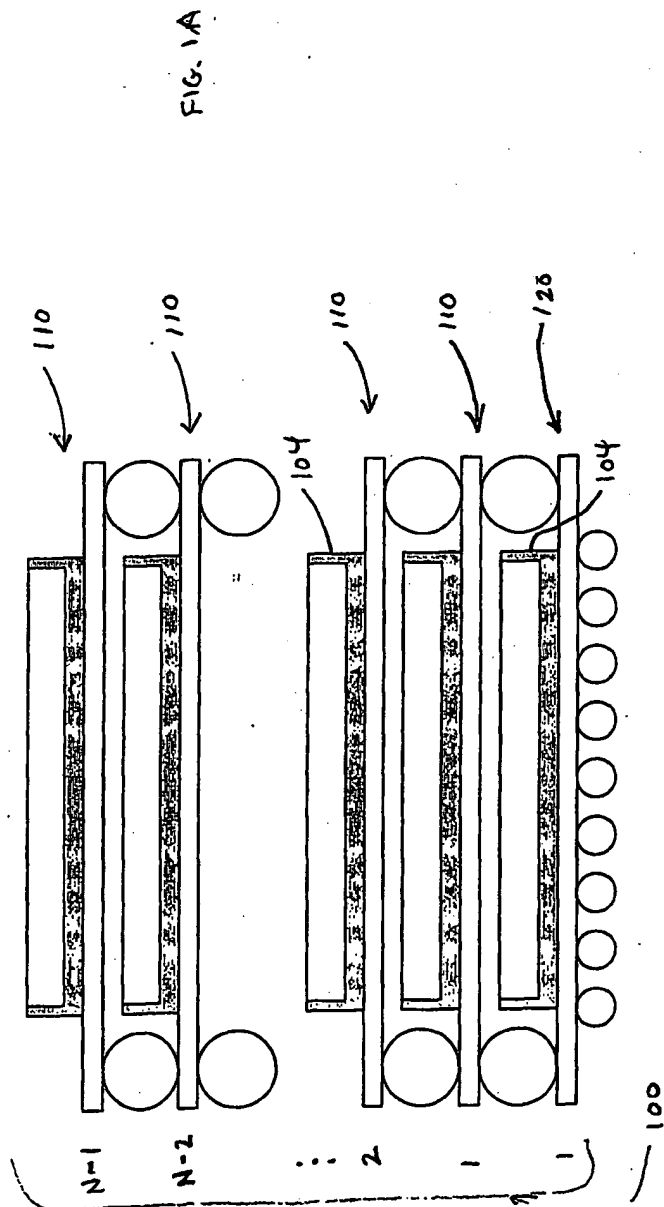


FIG. 1B

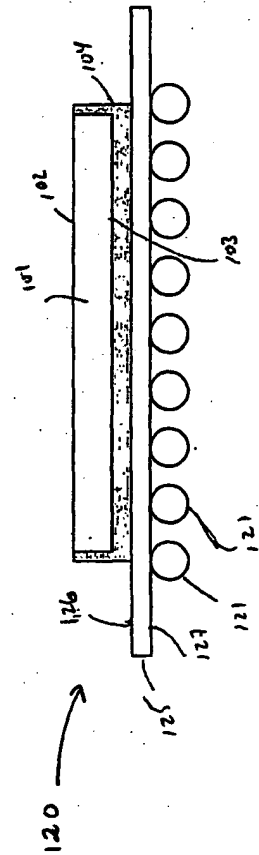


FIG. 1C

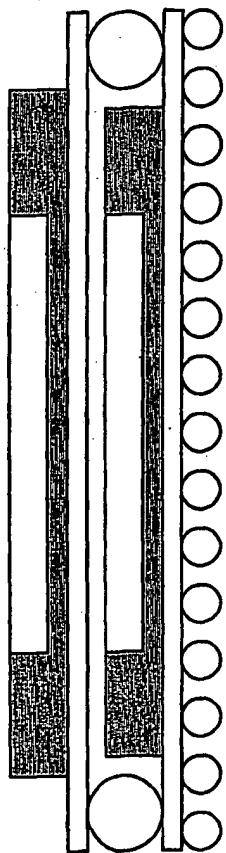


FIG. 2A

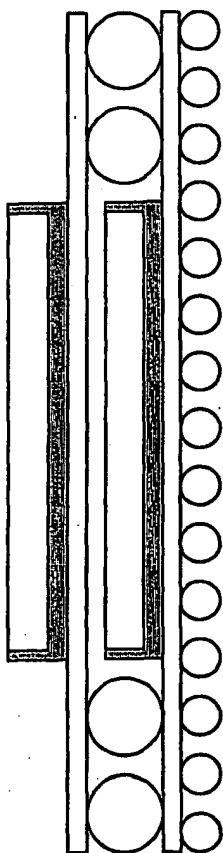


FIG. 2B

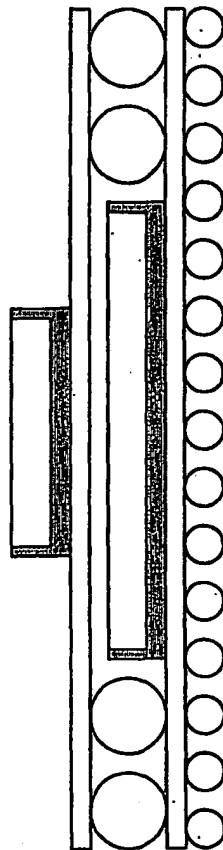
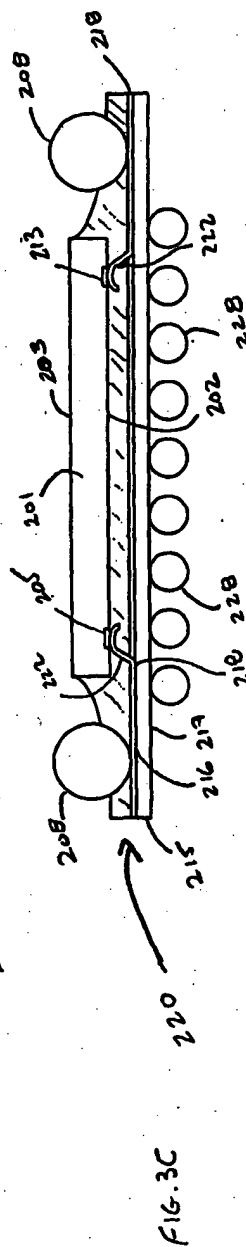
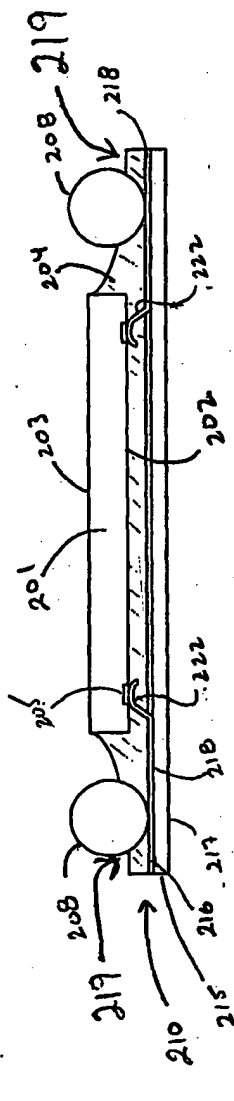
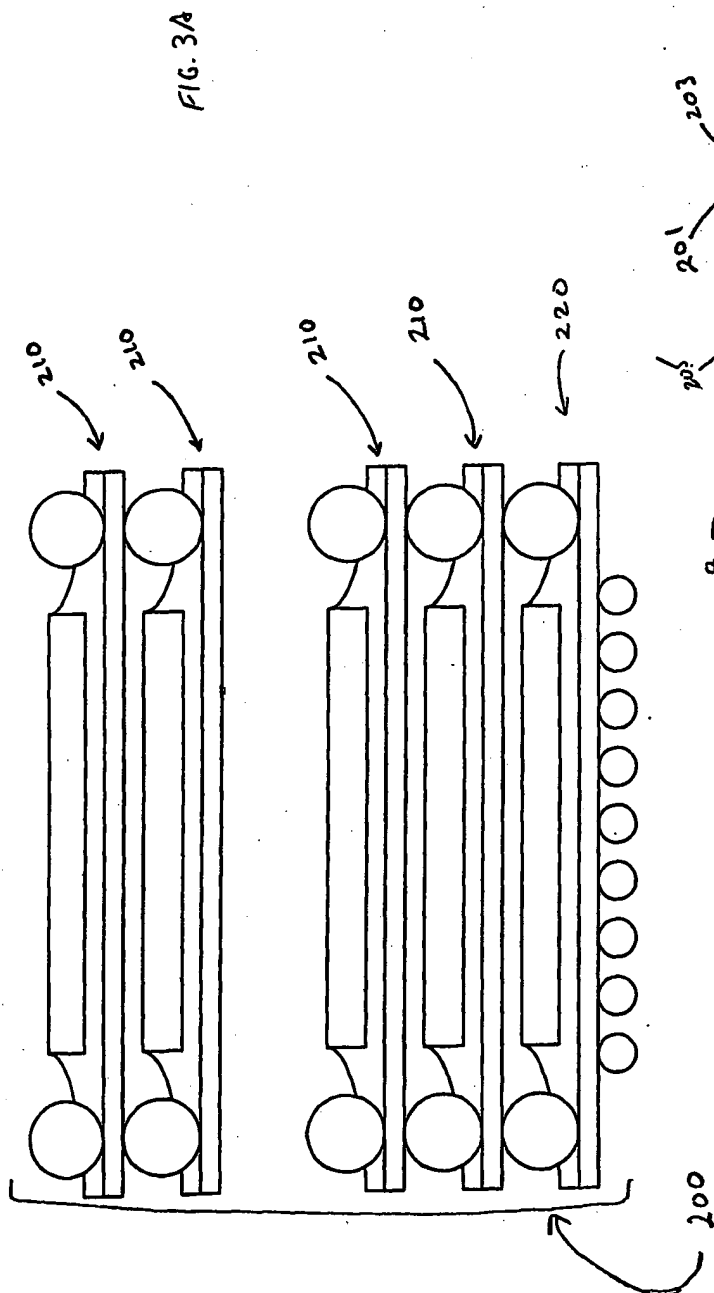


FIG. 2C



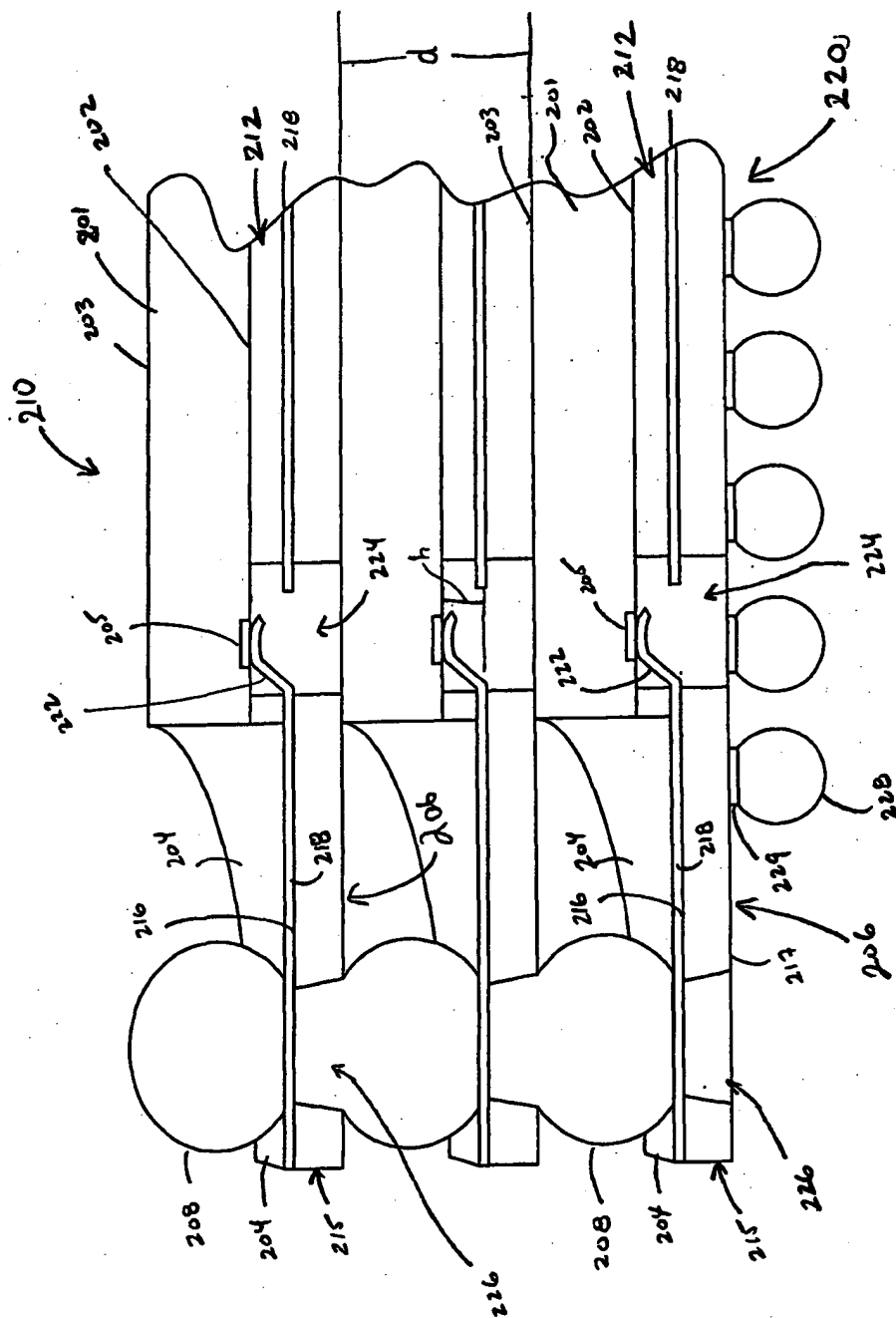


FIG. 4 A

FIG. 4C

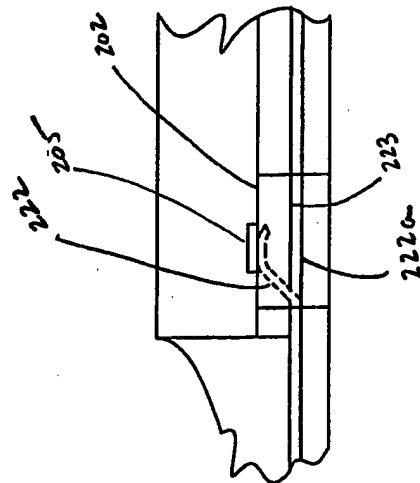
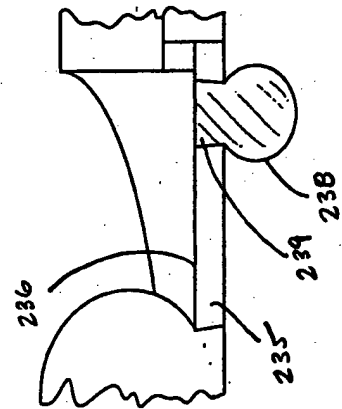


FIG. 4B



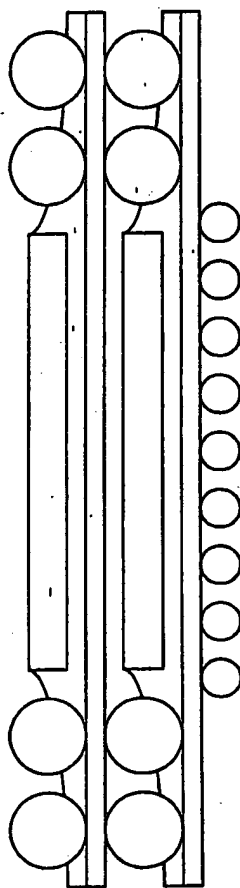


FIG. 5A

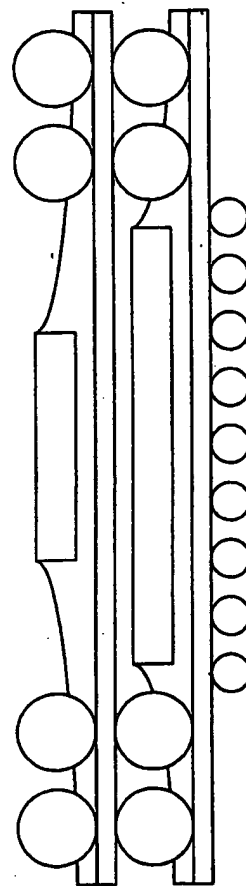


FIG. 5B

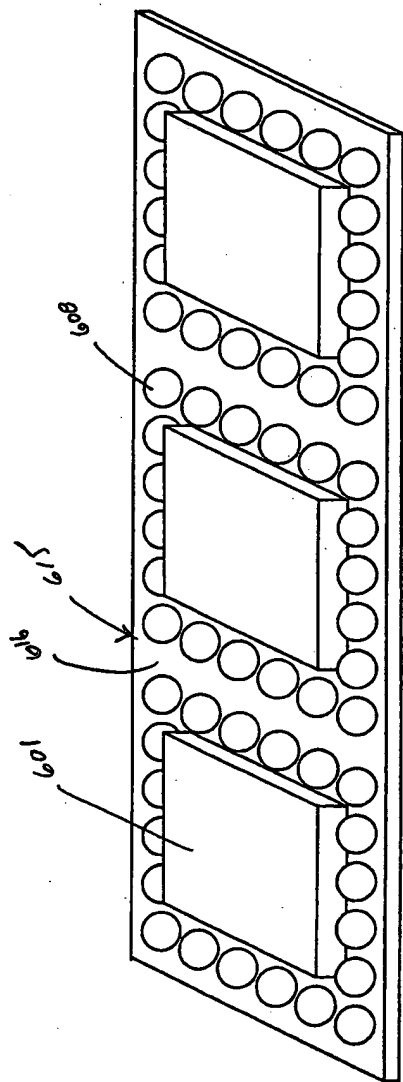


FIG. 6A

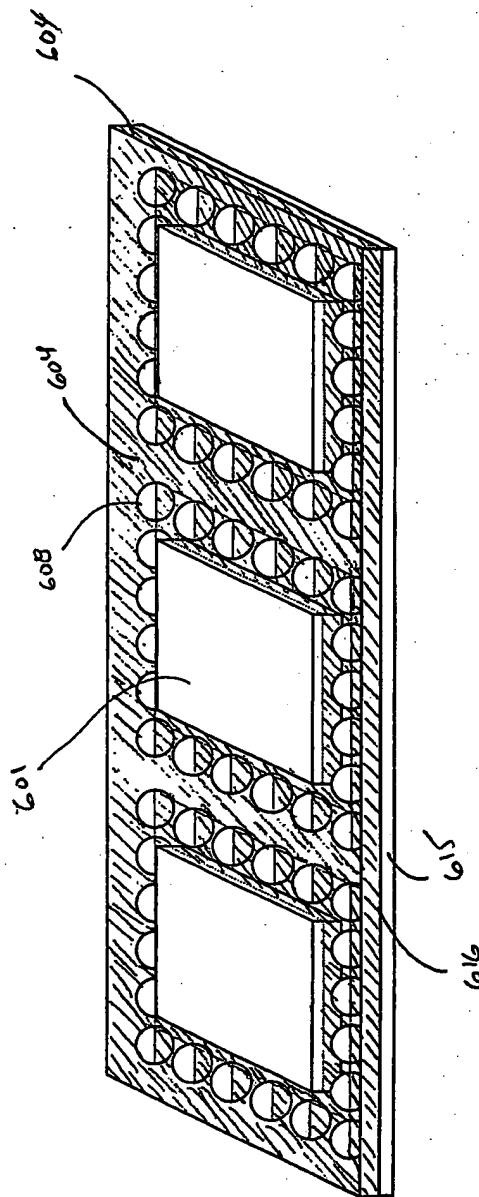
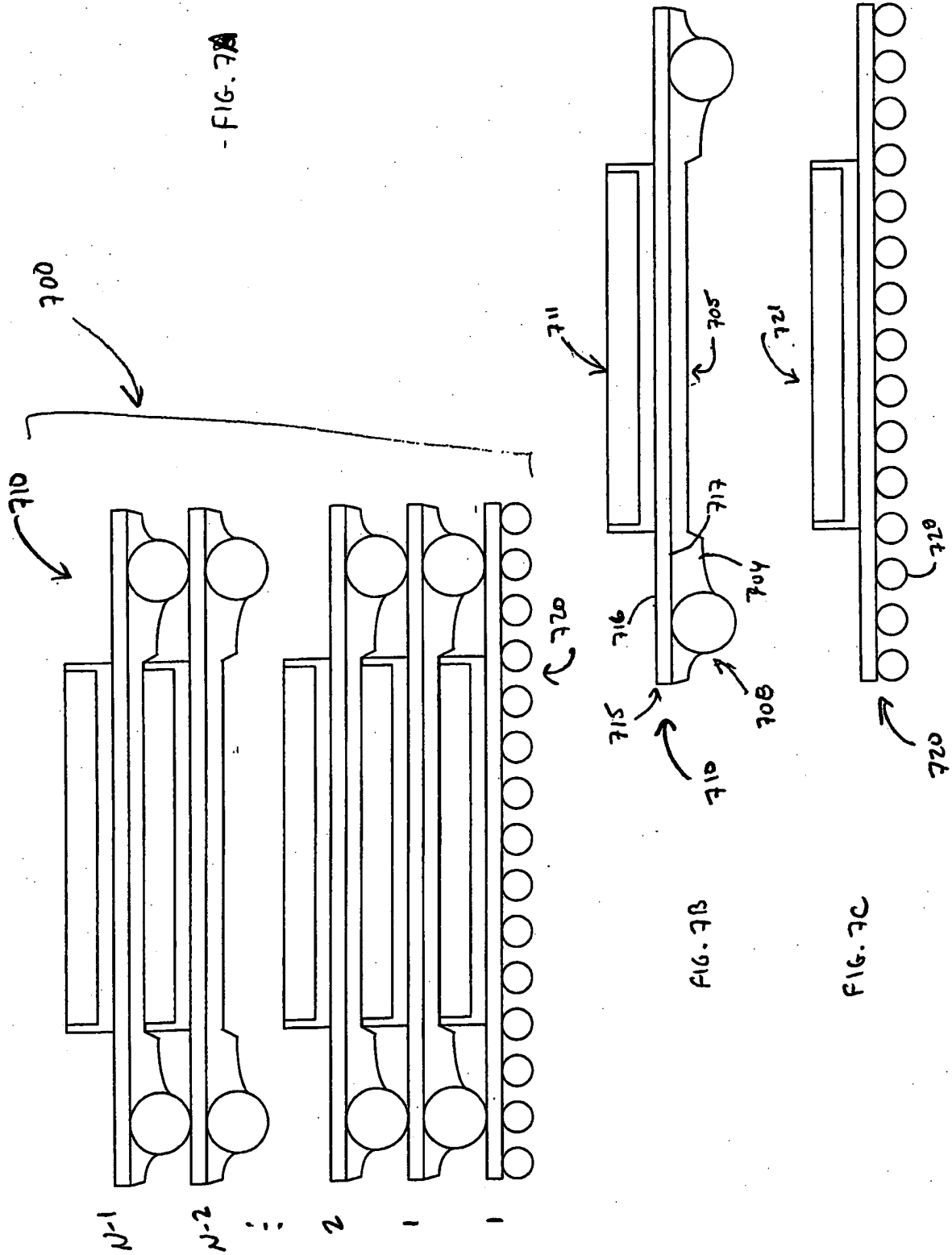


FIG. 6B



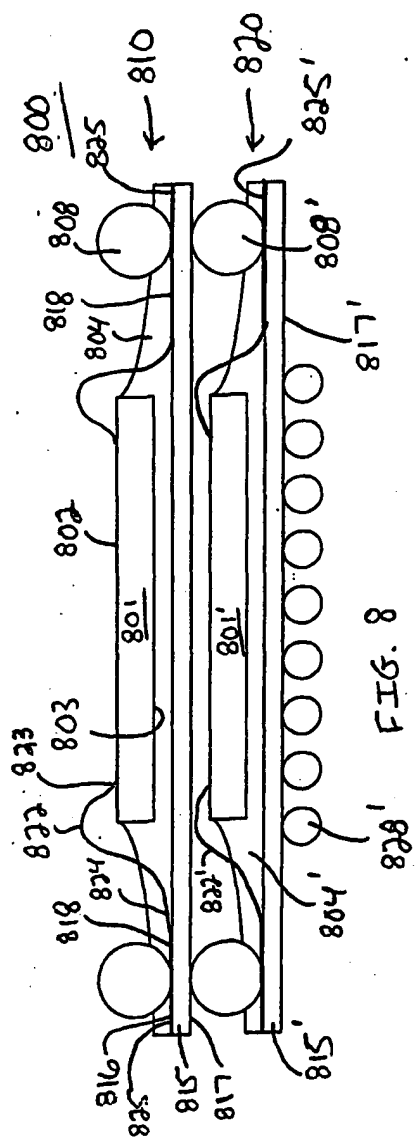
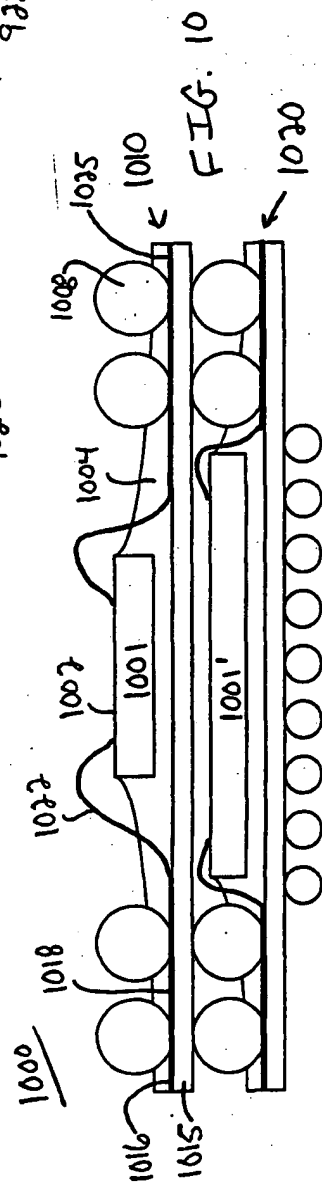
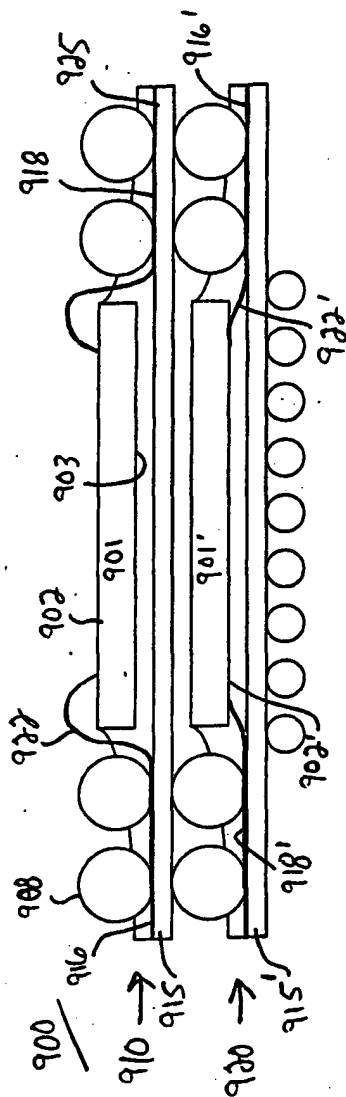


FIG. 9



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US02/26805

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 23/14, H01L 23/48

US CL : 257/702, 638, 680, 686, 723, 783, 784, 690

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/702, 638, 680, 686, 723, 783, 784, 690

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,763,939 A (Yamashita) June 9, 1998 (09-06-1998) Col. 3-10	1-28
Y	US 6,101,100 A (Londa) 8 August 2000 (08-08-2000), Column 3-6	1-28
Y	US 5,898,220 A (Ball) 27 April 1999 (27-04-1999), Column 4 and 5	1-28
Y	US 6,137,164 A (Yew et al) 24 October 2000 (24-10-2000), Column 2-8	1-28



Further documents are listed in the continuation of Box C.



See patent family annex.

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"T"

later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y"

document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"

document member of the same patent family

Date of the actual completion of the international search

28 September 2002 (28.09.2002)

Date of mailing of the international search report

07 NOV 2002

Name and mailing address of the ISA/US

Commissioner of Patents and Trademarks

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